PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/626,718
Filing Date	July 25, 2003
First Named Inventor	MIURA et al.
Art Unit	~~Unassigned~~ 2818
Examiner Name	~~Unassigned~~ LONG TRAN
Attorney Docket Number	500.33045CC3

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
LKT		US-4,839,306	06/1989	Wakamatsu	
LKT		US-4,842,675	06/1989	Chapman et al.	
LKT		US-4,860,070	08/1989	Arimoto et al.	
LKT		US-4,890,147	12/1989	Teng et al.	
LKT		US-5,079,181	01/1992	Shimizu et al.	
LKT		US-5,258,332	11/1993	Horioka et al.	
LKT		US-5,293,512	03/1994	Nishigoori et al.	
LKT		US-5,298,782	05/1994	Sundaresan	
LKT		US-5,329,138	07/1994	Mitani et al.	
LKT		US-5,332,683	07/1994	Miyashita et al.	
LKT		US-5,386,131	01/1995	Sato	
LKT		US-5,426,239	06/1995	Okumura et al.	
LKT		US-5,461,248	10/1995	Jun	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]–Number[4]–Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Country	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
LKT		JP 3-96249	04/1991	Japan (Abstract only)		
LKT		JP 3-236283	10/1991	Japan		
LKT		JP 4-127433	04/1992	Japan (Abstract only)		

OTHER DOCUMENTS

Miura et al., "Residual Stress Measurement in Silicon Substrates after Thermal Oxidation", JSME Int'l Journal, Series A, Vol. 36, No. 3, 1993, pages 302-308

Wolf, "Fully Recessed Oxide Locos Processes", Silicon Processing for the VLSI Era, Vol. II, page 28, 2.3

Saito et al., "Development of a Stress Simulation Program For Semiconductor Devices Considering Their Fabricating Process", Computational Mechanics '91 Proc. of Int. Conf. on Comp. Eng. Sci. 1991, pages 880-883

Saito et al., "A Two-Dimensional Thermal Oxidation Simulator Using Visco-Elastic Stress Analysis", IEDM, 1989, pages 695-698

Magdo et al., "Framed Recess Oxide Schme For Disclocation-Free Planar Si Structures", SOLID-STATE SCIENCE AND TECHNOLOGY, Vol. 125, No. 6, 1978, pages 932-936

Chiu et al., "A Bird's Beak Free Local Oxidation Technology Feasible for VLSI Circuits Fabrication", IEEE TRANSACTIONS ON ELECTRON DEVICES, Vo. ED-29, No. 4, 1983, pages 536-540

Examiner Signature	LONG TRAN	Date Considered	11/01/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard St.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.